

REMARKS

The title was objected to as not being descriptive. Applicants have amended the title and respectfully submits that the title is descriptive.

Claims 1-30 stand rejected under 35 USC § 102(e) as being anticipated by US Pat. No. 6,493,741 (hereafter Emer). Applicants have amended claims 1, 5, 6, 7, 12 - 18, 20-21, canceled claims 24 – 30 and added claims 31 and 32. Applicants respectfully submit that applicants' claims are distinguishable over Emer.

Emer discusses the use of a Quiesce mechanism to (possibly) idle a thread. However, Emer does not detail a situation in which multiple variables (e.g., lock variables) may be stored in a memory region monitored by monitor hardware.

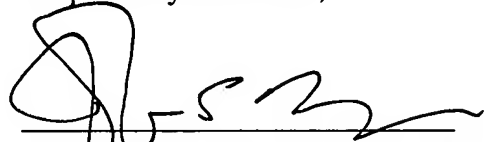
One example of an embodiment that uses the monitor mechanism to monitor values for two subtasks of a thread is discussed with regard to Figure 9c of applicants' specification. In this embodiment, two variables (CV1 and CV2) are stored in locations within the same cache line, allowing change in either variable to trigger the monitor mechanism. For example, in some embodiments, this may allow a thread to be inactivated until one of either of two lock variables can be obtained. Then, work associated with that variable may be commenced or continued. Thus, the monitor mechanism may be used in a new and efficient manner.

Applicant's claims read more broadly on such types of multi-variable usage models, but can likewise be appreciated to differ from the single lock variable checking Emer discusses. Moreover, Emer does not discuss the use of linear addresses, implicit operands, or mask operands.

Applicants submit that all claims now pending are in condition for allowance.
Such action is earnestly solicited at the earliest possible date. If there is a deficiency in
fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 1/3/05


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